

DESIGN OF LOW POWER TEST PATTERN GENERATOR

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ABSTRACT

Test pattern generator is more suitable for built in self test (BIST) structures used for testing of VLSI circuits. The objective of BIST is to reduce power dissipation. The main aim of the project is to design and implement design of low power test pattern generator (TPG) using LP-LFSR. LFSR and counter are designed with 14 transistor's D flip flop. This increases more power consumption and delay. Area occupied by the circuit is also large. The proposed test pattern generator reduces power consumption and delay. In this approach LFSR and counter are designed with 5 transistor D flip flop which reduces power consumption and delay. The proposed method is faster when compared to area and speed.

KEYWORDS: BIST, D Flip Flop, LFSR, Test Pattern Generator

I. INTRODUCTION

The main challenging areas in VLSI are performance, cost, testing, area, reliability and power. The demand for portable computing devices and communication system are increasing rapidly. These applications require low power dissipation for VLSI circuits. In general, the power dissipation of a system in test mode is more than in normal mode.

- Four reasons are blamed for power increase during test.
- High switching activity due to nature of test patterns
- Parallel activation of internal cores during test
- Power consumed by extra design-for-test (DFT) circuitry and Low correlation among test vectors.

This extra average and peak power consumption can create problems such as instantaneous power surge that cause circuit damage, formation of hot spots, difficulty in performance verification, and reduction of the product field and life time. Thus special care must be taken to ensure that the power rating of circuits is not exceeded during test application.

Flip-Flop is an electronic circuit that stores a logical state of one or more data input signals in response to a clock pulse. Flip-flops are often used in Computational Circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period. At each rising or falling edge of a clock signal, the data stored in a set of flip-flops is Circuitry. Delay Flip-Flop (DFF) has been the integral part of any digital system to construct the sequential part of it.

The XOR gate forms the basic building blocks of various digital VLSI circuits like full adder, multiplier, comparator and parity checker. Enhancing the performance of the XOR gates can significantly improve the performance of the system as whole. The design of this gate has been undergoing a considerable improvement in terms of power consumption. Many design architectures and techniques have been developed to reduce power consumption and has

become one of the primary focuses of digital design. This paper proposes a 5T XOR circuit which reduces the threshold-loss problem significantly as exists in previous designs and improves the power consumption too. The rest of the paper is organized as follows: In section-II analysis of power for testing is discussed. In section-III review of previous work is discussed. In section-IV proposed work is discussed. In section-V implementation details are discussed. In section-VI simulated outputs are shown and section-VII is the conclusion.

II. ANALYSIS OF POWER FOR TESTING

There are two major components of power dissipation in a CMOS circuit, one is Static power dissipation due to leakage current or other currents drawn continuously from the power supply and second was Dynamic power dissipation due to charging and discharging of load capacitances and short-circuit current. The following two subsections discuss about the individual power components.

1. Static Power Dissipation

The static (or steady-state) power dissipation of a circuit is given by the following expression:

$$P_{\text{STATIC}} = I_{\text{STATIC}} \cdot V_{\text{DD}} \quad (1)$$

Where I_{STATIC} is the current that flows between the supply rails in the absence of switching activity and V_{DD} is the supply voltage. Ideally, the static current of the CMOS inverter is equal to zero, as the positive and negative metal oxide semiconductor (PMOS and NMOS) devices are never ON simultaneously in the steady-state operation. However, there are some leakage currents that cause static power dissipation. The sources of leakage currents are Reverse-Biased pn Junction Leakage Current, Sub-threshold Leakage Current, Gate Leakage Current and Gate-Induced Drain Leakage Current.

2. Dynamic Power Dissipation

Dynamic power dissipation mainly depend upon two factors, one is due to Charging and Discharging of Load capacitors and second was due to Short-Circuit Current.

2.1 Charging and Discharging of Load Capacitors

For a CMOS inverter, the dynamic power is dissipated mainly due to charging and discharging of the load capacitance. When the input to the inverter is switched to logic state 0, the PMOS is turned ON and the NMOS is turned OFF. This establishes a resistive DC path from power supply rail to the inverter output and the load capacitor C_L starts charging, where as the inverter output voltage rises from 0 to V_{DD} . During this charging phase, a certain amount of energy is drawn from the power supply. Part of this energy is dissipated in the PMOS device which acts as a resistor, whereas the remainder is stored on the load capacitor C_L .

During the high-to-low transition, the NMOS is turned ON and the PMOS is turned OFF, which establishes a resistive DC path from the inverter output to the Ground rail. During this phase, the capacitor C_L is discharged, and the stored energy is dissipated in the NMOS transistor. In summary, each switching cycle (consisting of an L to H and H to L transition) takes a fixed amount of energy, which is equal to

$$C_L V_{\text{DD}}^2 \quad (1)$$

In order to compute the power consumption, we have to take into account how often the device is switched. If the inverter is switched on and off during a given time period, the power consumption is given by,

$$P_D = C_L \cdot V_{\text{DD}}^2 \cdot f_O \quad (2)$$

Where f_0 represents the number of rising transitions at the inverter output per second.

2.2 Short-Circuit Current

Even though under the simplifying assumption of zero rise and fall times for NMOS and PMOS devices for static CMOS logic gates, there exists no direct current path between the power and ground rails, a more realistic timing model for CMOS technology reveals that the input switching is gradual and not abrupt. Consequently, during switching of input, the PMOS and NMOS devices remain ON simultaneously for a finite period.

The current associated with this DC current between supply rails is known as short-circuit current (ISC). Since short-circuit power is delivered by the voltage supply V_{DD} , the total power can be written as,

$$P_{SC} = I_{SC} \cdot V_{DD} \quad (3)$$

So the total power consumption of the CMOS inverter is now expressed as the sum of its three components:

$$P_{TOTAL} = P_{STATIC} + P_D + P_{SC} \quad (4)$$

In typical CMOS circuits, the capacitive dissipation was by far the dominant factor. However, with the advent of deep-submicron regime in CMOS technology, the static (or leakage) consumption of power has grown rapidly and account for more than 25% of power consumption in SoCs and 40% of power consumption in high performance logic.

So it can be easily found that the power consumption depends on the switching activities for a fixed circuit structure, voltage and fixed clock frequency. The switching activities can be reduced by inserting 2^m vectors between two neighboring seeds, in which each vector has only one bit difference with the last vector, thus pseudo random single input changing vectors are generated.

BIST Approach

BIST is a design for testability (DFT) technique in which testing is carried out using built-in hardware features. Since testing is built into the hardware, it is faster and efficient. The BIST architecture shown in figure.1 needs three additional hardware blocks such as a pattern generator, a test controller. For pattern generator we can use either a ROM with stored patterns, counter, or a linear feedback shift register (LFSR).

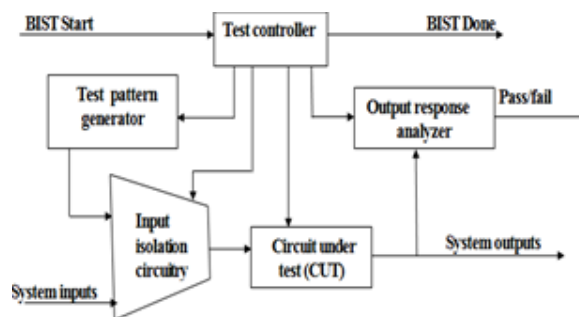


Figure 1: BIST Basic Block Diagram

Classification of Test Strategies:

1. Weighted Pseudorandom

In weighted pseudorandom testing, pseudorandom patterns are applied with certain 0s and 1s distribution in order to handle the random pattern resistant fault undetectable by the pseudo random testing thus, the test length can effectively shortened.

2. Pseudo Exhaustive Testing

Pseudo exhaustive testing divides the CUT into several smaller sub circuits and tests each of them exhaustively. All detectable flows can be detected.

3. Pseudorandom Testing

Pseudorandom testing involves application of certain length of test patterns that have certain randomness property. The test patterns are sequenced in a deterministic order.

4. Exhaustive Testing

Exhaustive testing involves the application of all possible input combinations to the circuit under test (CUT).

5. Stored Patterns

Stored patterns approach tracks the pre-generated test patterns to achieve certain test goals. It is used to enhance system level testing such as the power-on self test of a computer and microprocessor functional testing using micro programs.

III. REVIEW OF PREVIOUS WORK

Because of simplicity of the circuit and less area occupation, linear feedback shift register [LFSR] is used at the maximum for generating test patterns. LP-TPG structure consists of modified low power linear feedback shift register (LPLFSR), m-bit counter; gray counter, NOR-gate structure and XOR-array. The m-bit counter is initialized with Zeros and which generates 2^m test patterns in sequence.

The m-bit counter and gray code generator are controlled by common clock signal [CLK]. The output of m-bit counter is applied as input to gray code generator and NOR-gate structure. When all the bits of counter output are Zero, the NOR-gate output is one. Only when the NOR-gate output is one, the clock signal is applied to activate the LP-LFSR which generates the next seed. The seed generated from LP-LFSR is Exclusive-ORed with the data generated from gray code generator. The patterns generated from the Exclusive-OR array are the final output patterns.

In this project test pattern generator is implemented using LFSR, counter and XOR gate. LFSR is the interconnections of D flip flops and XOR. Counter is designed by using D flip flop. And XOR gate is implemented by using 12 transistor D flip flop. Each D flip flop have four transistors and two inverters. Totally the D flip flop consists of 36 transistors. Simulation and analysis are carried out in HSPICE model.

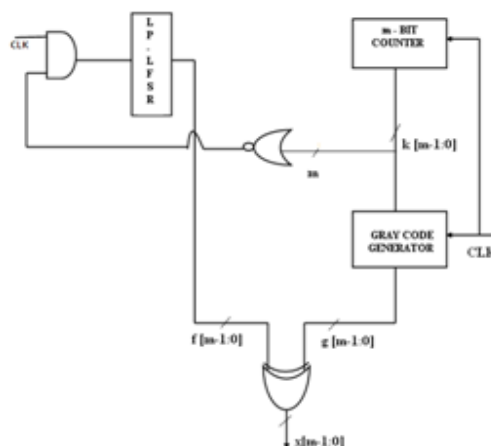


Figure 2: Low Power Test Pattern Generator

IV. PROPOSED WORK

In test pattern generator linear feedback shift register (LFSR), counter, gray code and XOR gates are designed. LFSR is the combination of D flip-flops and XOR gates. LFSR and counter are implemented using D-flip flop and gray code is implemented using 3 XOR gates. The traditional CMOS based Flip-Flop uses 36 transistors. Later a Latch was developed using 5 transistors where 3 NMOS transistors and 2 PMOS transistors are used for the design. The schematic of flip-flop is shown in Figure 3

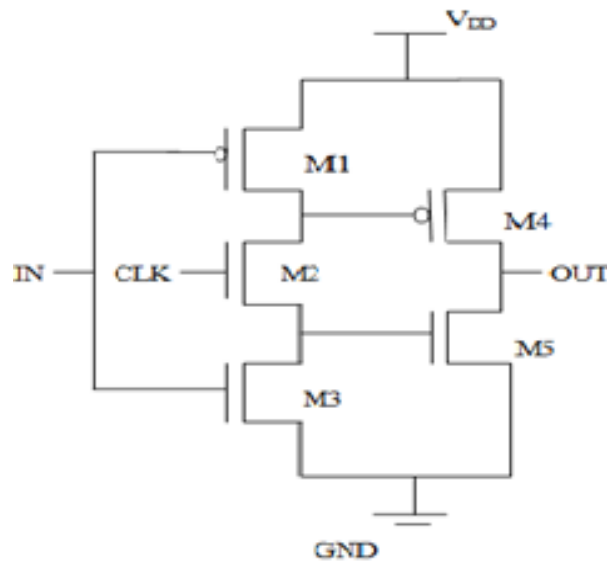


Figure 3: 5 Transistor Flip Flop

When CLK and input IN are high then the transistors M1, M5 are OFF and remaining transistors M2, M3, M4 are ON. The output becomes high. During ON clock period whatever is the value of input it becomes output. It also acts as a Flip-Flop when the input IN has less pulse width. The purpose of LFSR is to generate test patterns which are used in the BIST circuits.

V. IMPLEMENTATION DETAILS

To validate the effectiveness of the proposed method we select the performance of LFSR and counter and 5 transistor flip flop. Simulation and analysis is carried out with HSPICE.

Table 1: Power, Delay and PDP for LFSR

OUTPUT NODES	POWER (μm)	DELAY (ns)	PDP (POWER*DELAY) (fj)
4	5.10×10^{-04}	58.22	0.029
5	5.10×10^{-04}	51.40	0.026
6	5.10×10^{-04}	51.66	0.026
7	5.10×10^{-04}	61.83	0.0199

Table 2: Power, Delay and PDP for Counter

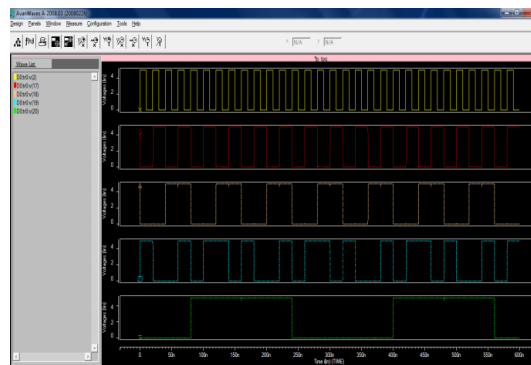
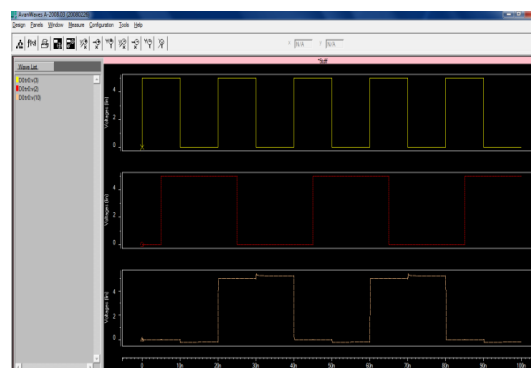
OUTPUTNODES	POWER (μm)	DELAY (ns)	PDP (POWER*DELAY) (fj)
5	5.10×10^{-04}	51.86	0.022
7	5.10×10^{-04}	47.69	0.024
10	5.10×10^{-04}	48.90	0.024
12	5.10×10^{-04}	39.11	0.0199

Table 3: Average Power for LP-TPG and XOR

DESCRIPTION	LP TPG	XOR
AVERAGE POWER	4.432×10^{-4}	2.39×10^{-4}
MAXIMUM POWER	0.1441	0.1056

From the implementation results, it is verified that the proposed method gives better power reduction and delay when compared with the existing method.

VI. SIMULATED OUTPUT WAVEFORMS

**Figure 4: Simulated Output for LP-LFSR****Figure 5: Simulated Output for XOR**

VII. CONCLUSIONS

A low power test pattern generator has been proposed which consists of modified D flip flop and XOR gate. This reduces the power delay and area of the circuit. From the implementation results it is verified that the proposed method gives 51 percent of delay reduction compared to the existing method.

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